Evaluating Energy and Delay of DICE and PDICE SRAM Cells at 32nm Technology

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***Abstract*—At nanometer nodes, with the reduced voltage due to technology scaling, soft errors due to cosmic rays can affect electronic devices even on earth. This work presents the design evaluation of two robust SRAM Cell, DICE [1] and PDICE [1], evaluating the timing and power characteristics on a nanometer technology. These cells are recognized by the radiation robustness, however with a penalty on the transistor number and, consequently on the power and timing. This work helps the designers to know better these circuits behavior. After the simulations, DICE presents the lowest read time.**

***Index Terms*—SRAM, nanotechnology, DICE, PDICE**

I. Introduction

Processors performance are continuously speeding up due to pipeline and branch predictors techniques. However, the memory system still being a significant issue on the processors performance evolution. Historically, the insertion of cache levels designed with SRAM (Static Random Access Memory) cells in the same processor technology node allowed to executed data and instructions access in a cycle of the clock, instead of the high time to access data from the hard drive memory. Cache design influence significantly the total system performance, that demands area, timing, and power optimization.

With the technology scaling, the area has no longer been a really significant problem, allowing large integration scale of cache levels inside the processors chip. However, power consumption rises as high claiming for many applications. Moreover, the aggressive scaling alongside the low supply voltages, large transistor density, and the high-frequency operation introduce new reliability issues, such as the high radiation effects sensitivity and multi-charge collection [2], [3].

During a long period, the radiation effects in electronic systems were only considered relevant in cases of military, avionic or spatial designs. However, with microelectronics advancement, radiation-induced faults can occur even at earth level [4]. The soft errors are the consequence of a transient pulse generated by the interaction of energetic particles near a sensitive region of a transistor when the collected charge (Q_{coll}) exceeds the critical charge (Q_{crit}). According to the energy of ionized particles hitting the silicon, the incident angle and the impact site, transient pulses can cause minor perturbations or even critical failures in the system behavior [5]. The main effects on memory elements are classified as Single Event Upsets (SEU) and are characterized as the occurrence of a bitflip on the memory element.

There are few hardened memory solutions on the literature, with particular reference to the CMOS DICE (Dual Interlocked Storage Cell) [1] [6] mainly because the reduced increase on the are compared to traditional replication techniques as triple module redundancy (TMR). DICE cell consists of two transistor groups whose layout on the crystal increases the cell stability against the impact of single particles. A fault of the cell state does not take place if the particle impacts transistors of one group only.

This work is the first part of a project that aims to evaluate DICE cells and related work, as PDICE cell [1], about radiation robustness in nanotechnologies, considering CMOS bulk nodes, SOI devices and FinFET devices. The main objective of this project is to provide information about the current radiation robustness memory solutions always comparing with traditional SRAM cell designs, providing electrical characteristics of the evaluated cells to allow designers to trace tradeoffs in the SRAM cell decision for different sets of applications.

Thus, this work explores the memory cells 6T, DICE and PDICE, shown in Figure1 and 2, investigating the impact on timing and power of these well-known hardened memory cells. All the evaluations consider the electrical behavior to show the cost inserted in the design when radiation robustness is mandatory.

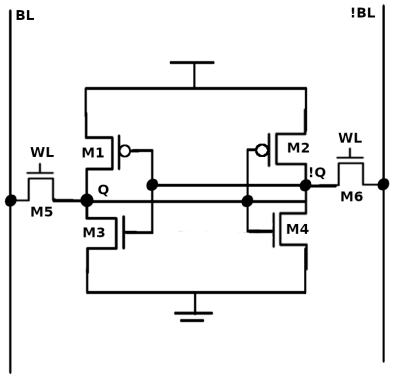
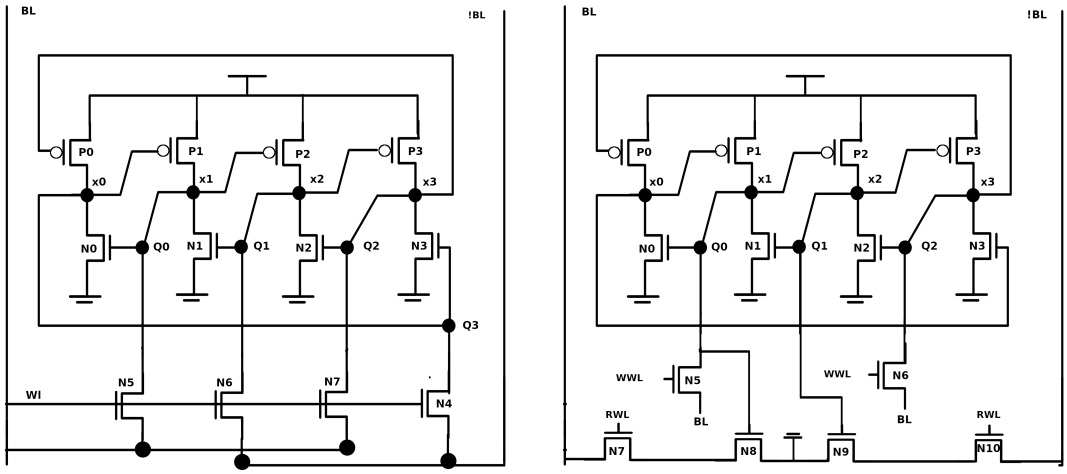
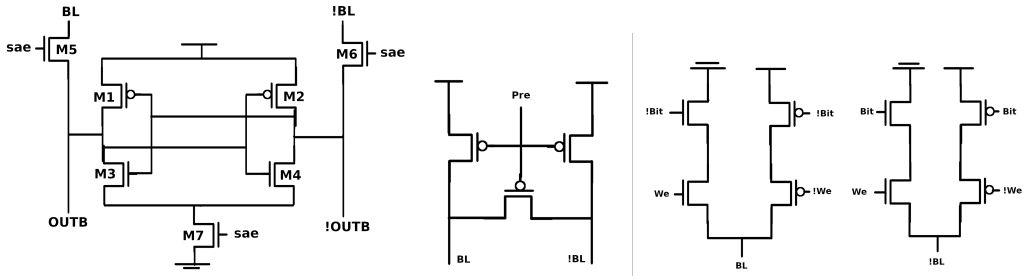


Fig. 1: 6T SRAM Cell



(a) DICE (b) PDICE

Fig. 2: Hardened SRAM Cells



(a) 6T Read Circuit (b) Pre-Charge Circuit (c) Write Circuit

Fig. 3: Complementary circuits

II. Robust SRAM topologies

The 6T cell is the most frequently used SRAM Cell on L1 cache design. DICE and PDICE cells are references on reliability SRAM designs. The three cells contain the Write and Pre-Charge circuits, found in the structure of SRAM architecture, and the 6T still has a Read Circuit. All these components takes the width (W) as 210nm, and their descriptions are in Figure 3. The 6T is composed of six transistors. The two most external to the cell are responsible for controlling of the access bitlines (BL-BLB) to internal nodes (Q-QB). Its control is given through the signal sent by Wordline (WL). These transistors are of the NMOS type and are called M5-M6. The internal part of the cell has two transistors of the PMOS type, that has the function of raising the logical value of the cell, referred to M1-M2, and two other NMOS transistors by decreasing the logical signal, called M3-M4.

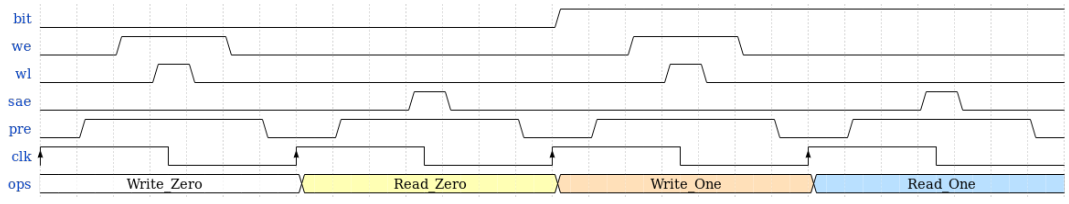
The DICE contain twelve transistors, which eight are used as inverter (P0-N0, P1-N1, P2-N2, P3-N3). Each inverter is connected with it's next and previous in the gate by the internal node X_i generating the robustness in the Hold. An example is X_0, if it's contain the logic value one will open P1 and close N3, so the internals nodes X_1 and X_3 will receive the logical values zero and one respectively.

The PDICE [1], which contain fourteen transistors, have better robustness than DICE, that means a resistance in Hold, Read and Write operations. That aspect comes from the independence between read and write, since there are two signals Read Wordline (RWL) and Write Wordline (RWL) instead of Wordline (WL).

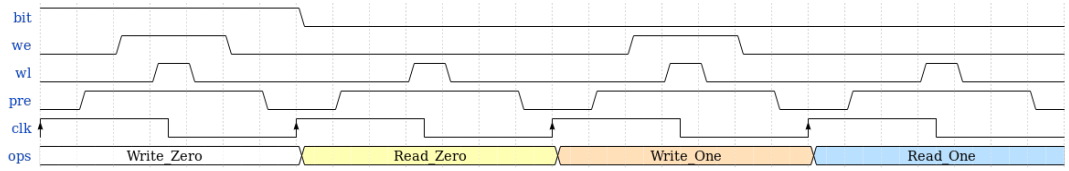
III. Methodology

In this work, all evaluation was done through electrical simulations using NGSpice Tool. The circuits were described in the SPICE language, using the model of HP (High Performance) in 32nm, operating at reference voltage of 0.9V [7].

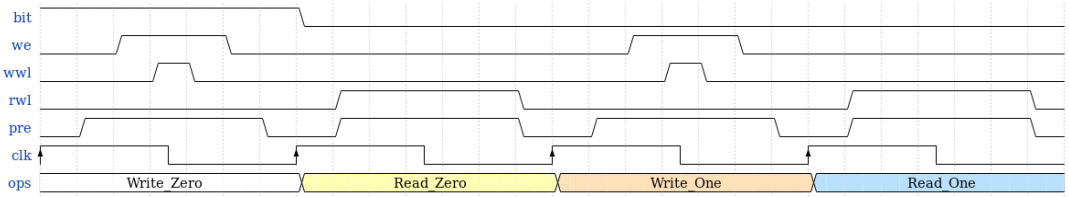
This work defines a sequence of operations that would allow to achieve reading and writing times, as well as energy consumption. The waves for each simulation are found in Figure 4. Initially, a write operation of the logical value 0 and, after a period of Hold, the value is stored is read. Subsequently, the writing of the logical value 1 is performed. Again, after a period of hold, the value stored is read. With the PDICE, was necessary add a voltage boost ($V_{boost} = 0.6V$) for writing the value zero and this value was found after several attempts, whose dynamics was the simulation of operations separately



(a) 6T Simulation



(b) DICE Simulation



(c) PDICE Simulation

Fig. 4: Simulation Details of the Write 0 / Read 0 / Write 1 / Read 1 operation sequence

and then a complete until encounter a adequate V_{boost} to perform all functions of a SRAM cell correctly.

Given an example of functioning, the waves of DICE, found in Figure 4, are segmented in two operations, which are writing and reading. The difference to write zero and one is described in the respective subsection, the same was done to read. Because of variation in the structure present in 6T and the two others SRAM cells, the value of bitlines to write are reversed for 6T. Likewise, the reading vary in which bitline is taken to verify the stored value. The PDICE waveform is the same as the DICE, except for the signal wl, that is split in rwl and wwl which are set when occurs write or read respectively. To write zero, the signal wl must be one to access the DICE cell. Afterwards, the signals BL and !BL needs to be one and zero respectively, and to achieve these values bit and we needs to be one, the same case for the signal pre, that used to pre-charge the bitlines (BL,!BL) before the writing. The change to write one lies in the reverse values of the bitlines made by the signal bit, which must to be zero. As well as writing, the wl must have one. Later, both bitlines have to be one and the signal pre produce that and the fall voltage of BL or !BL is required, the percentage and which bitline per stored logical value is described in the Table II. To measure the time for write and read, the voltage of signals and bitlines(BL-BLB) was used and the percentages are described in the Table I and II respectively.

The evaluation of the energy considers the total energy consumption of each SRAM circuit, for the total sequence write0/read0/write1/read1, which operation have one cycle of clock (clk).

TABLE I: Measures of Writing

Topology	Writing 0		Writing 1	
	Rise voltage	Fall Voltage	Rise voltage	Fall Voltage
6T	$wl * 0.5$	$q * 0.5$	$wl * 0.5$	$q * 0.5$
Dice	$wl * 0.5$	$q3 * 0.5$	$wl * 0.5$	$q3 * 0.5$
PDice	$wwl * 0.5$	$x0 * 0.5$	$wwl * 0.5$	$x0 * 0.5$

TABLE II: Measures of Reading

Topology	Reading 0		Reading 1	
	Rise voltage	Fall Voltage	Rise voltage	Fall Voltage
6T	$wl * 0.5$	$bl * 0.9$	$wl * 0.5$	$blb * 0.9$
Dice	$wl * 0.5$	$blb * 0.9$	$wl * 0.5$	$bl * 0.9$
PDice	$rwl * 0.5$	$bl * 0.6$	$rwl * 0.5$	$blb * 0.9$

IV. Results

The timing and power behavior of all the three cells were obtained. Figure 5 present the read and write times observed for the evaluated cells, and Figure 6 shows the energy results obtained considering all the energy consumption to the integrated operation sequence. These results are available in Table III for each operation to compare all SRAM cells.

The 6T cell presented contain a reading time greater than the writing time, mainly considering the write 0 operation. However, DICE cells also presents good timing results compared to 6T. Considering the critical times, the worst delay for DICE cell (8.6ps) is only 6% superior of 6T cells.

As expected, 6T cell have a shorter time for operations in the majority of the operations. However, the DICE is better than 6T to read and consumes less energy. The energy reduction is about 9%, even though the DICE cells has a significant number of devices, twice the number of 6T devices. Considering

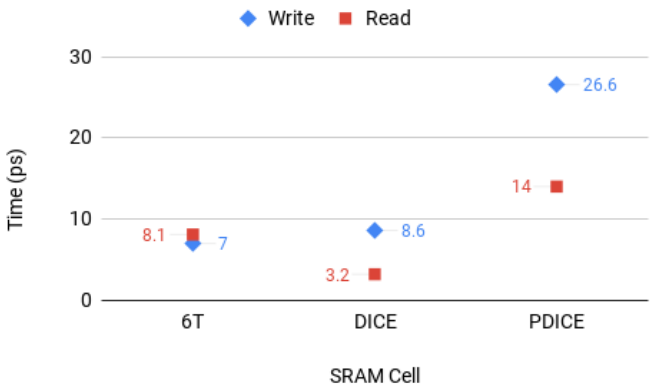


Fig. 5: Write and Read Times

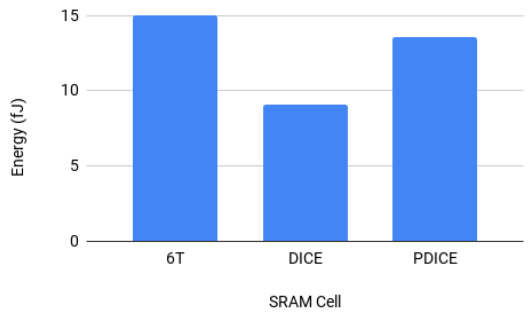


Fig. 6: Energy Consumption

energy, the same case occurs when comparing DICE and PDICE cells. The PDICE cells presents superior times per operations (superior to 3x of time degradation compared to 6T cell) and approximately 50% of energy increase.

TABLE III: Time and Energy Results

SRAM cell	Write0 (ps)	Read0 (ps)	Write1 (ps)	Read1 (ps)	Energy (fJ)
6T	3.8	8.0	7.0	8.1	11.1
DICE	5.2	3.2	8.6	2.1	10.1
PDICE	26.6	14	12.4	6.9	13.6

Table IV emphasizes the comparative evaluation of these cells with the adoption of a figure of metric described by the Equation 1 , where i and j represent different SRAM cells and C_i a time or energy for the respective cell. The most significant difference is between PDICE and DICE, which in all measures the PDICE is worse, proving the cost of robustness and having a higher number of transistors.

$$Compare_{ij} = (\frac{C_i}{C_j} - 1) * 100 \quad (1)$$

V. Conclusion

This work provides a comparison between the 6T, DICE and PDICE SRAM cells. The operating times and energy consumed by both topologies were evaluated. Through the analysis of the results, it was possible to verify a difference on the timing between the cells. The PDICE presents a higher time for the writing operation, being 280.00% and 208.94% slowest than the 6T and DICE respectively. In the reading operation, the DICE had a better performance than the others and PDICE was the worst. These data are illustrated in Figure 5. In terms of energy consumption, the DICE cell consumed about 39.33% and 33.09% less energy than 6T and PDICE. The graph in Figure 6 show this value.

TABLE IV: Comparison between SRAM cells

$(Cell_i, Cell_j)$	Write(%)	Read(%)	Energy(%)
(DICE,6T)	23.00	−60.49	−39.33
(PDICE,6T)	280.00	72.84	−9.33
(PDICE,DICE)	208.94	337.50	49.45

Such as 6T got the greater consumption of energy, which was not expected, that will be researched with an analysis in circuit behavior during write and read operations.

This first step on the main project shows how the DICE cell introduces robustness without timing degradation. As a future step, these cells will be evaluated about the linear energy transfer threshold to compare the radiation robustness of them. Also, next steps include the complete evaluation of these cells on SOI and FinFET technology.

VI. Acknowledgment

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